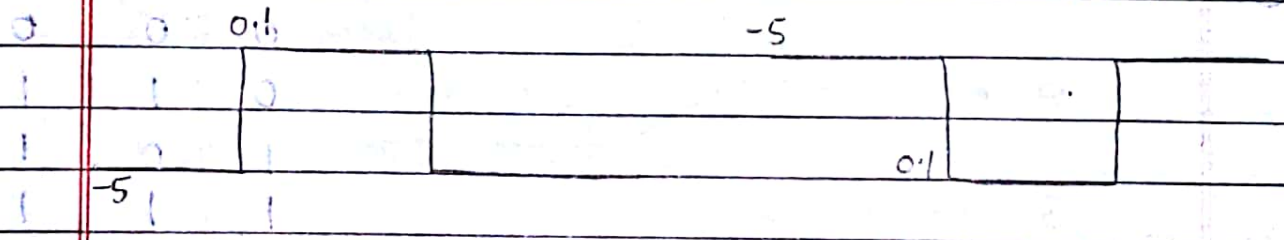
Unit - 1.

Positive Logic System

The system in which the most positive voltage shows high state i.e 1 (one) and most negative voltage shows low state i.e 0 (zero) is called 'Positive Logic System'.

Negative Logic System

The system in which most negative voltage shows high state and most positive voltage shows low state is called 'Negative Logic System'.

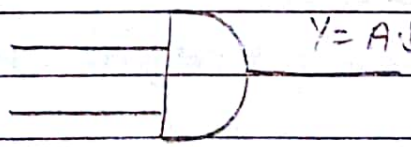


Positive Logic System

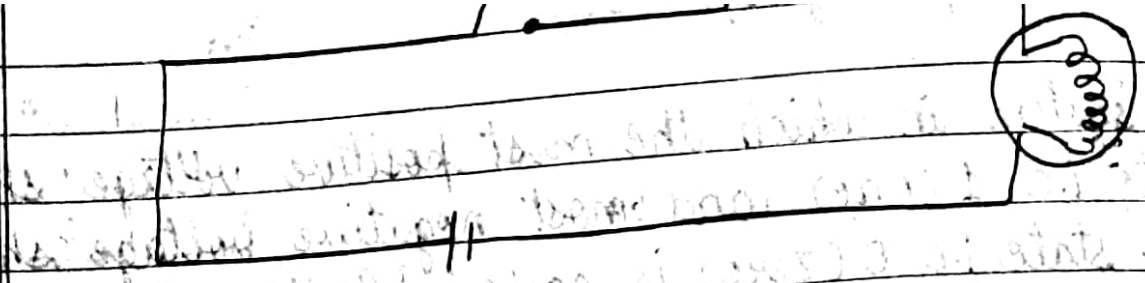
Negative Logic System

Basic Logic Gates

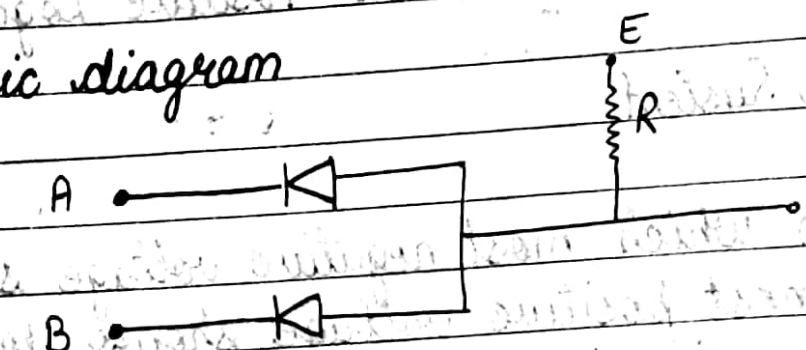
1. AND Gate



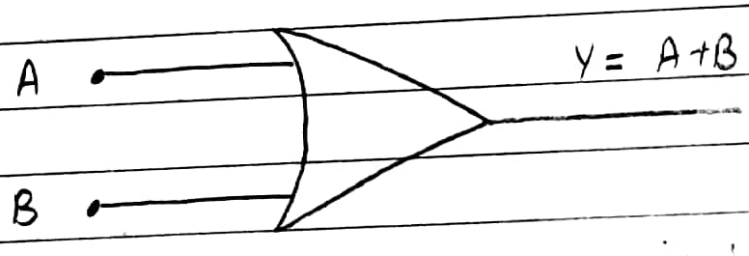
A	B	A·B = Y
0	0	0
0	1	0
1	0	0
1	1	0



Logic diagram

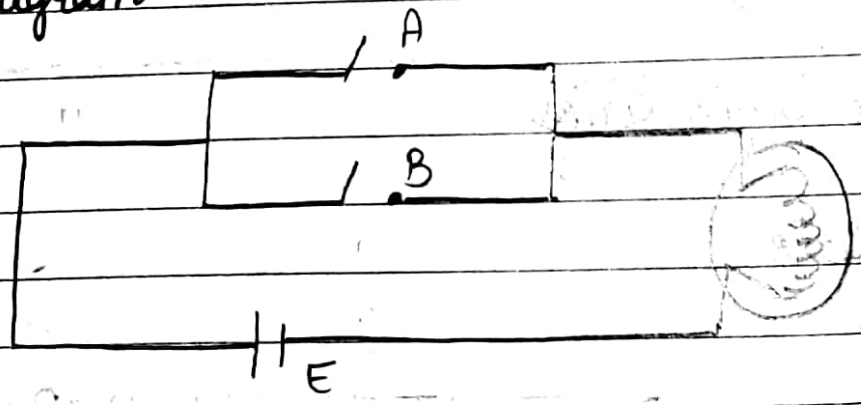


② OR Gate

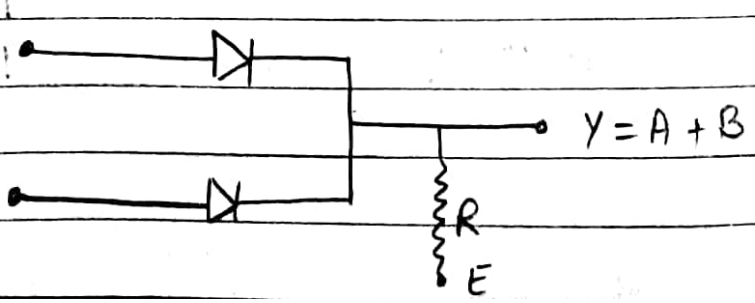


A	B	A+B=Y
0	0	0
0	1	1
1	0	1
1	1	1

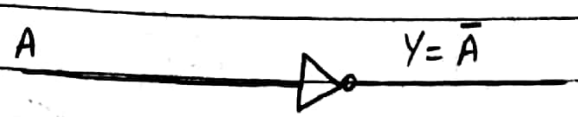
Switch Diagram



Logic Diagram



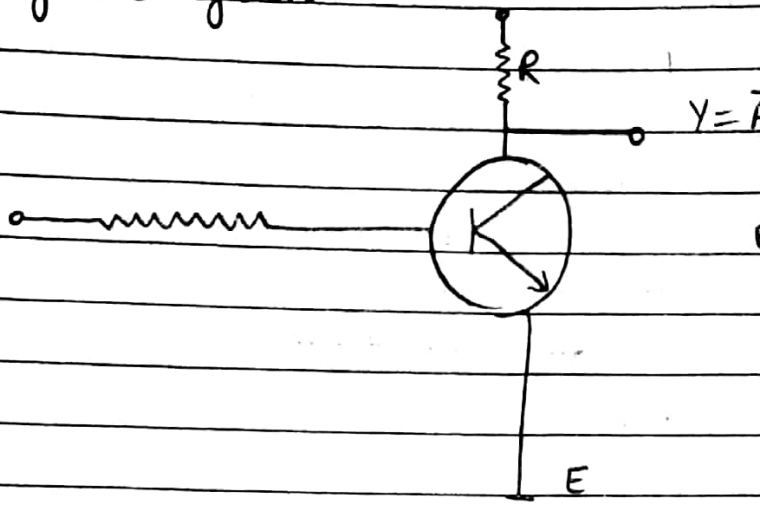
Not Gate



∴ Ā = compliments of A

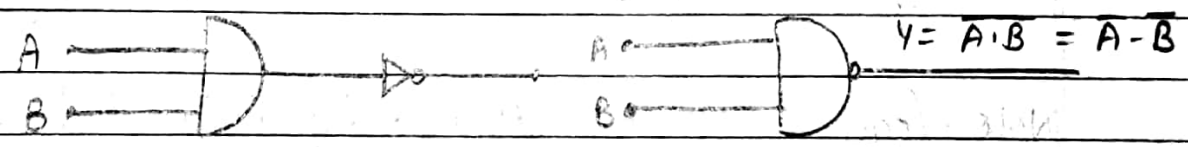
A	Y = Ā
0	1
1	0

Logic Diagram



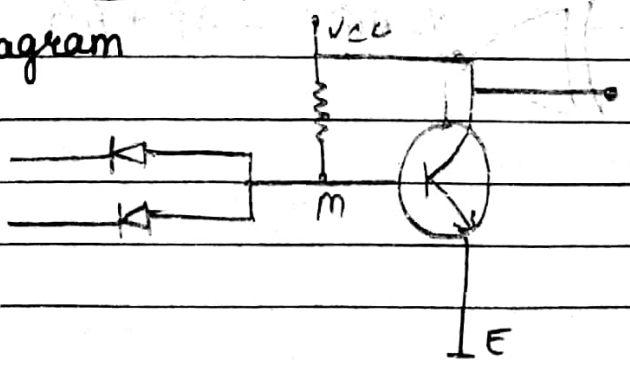
Universal Gates

NAND → (Not + And)

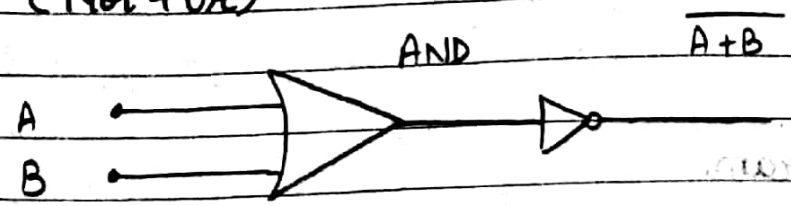


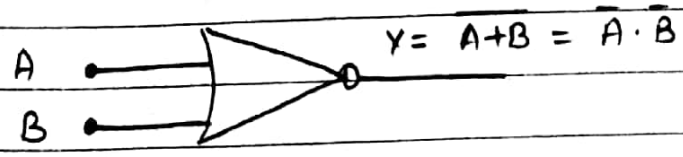
A	B	Y = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	1

Logic Diagram

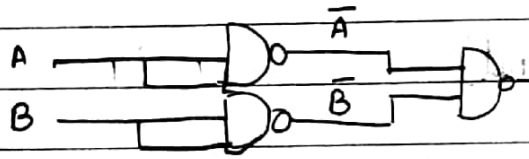


② NOR (Not + OR)





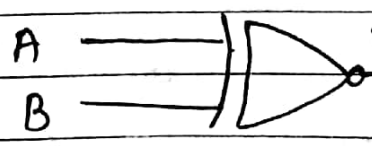
A	B	$Y = A+B$
0	0	1
0	1	0
1	0	0
1	1	0



$= \quad =$
$Y = \bar{A} + \bar{B}$
$Y = (A+B)$ [OR Gate]

Note : Logic Gates are formed by diodes & transistors
3 NAND gates make 1 OR gate.

Exclusive - OR Gate (Ex OR Gate)
The logic gate which gives low state when all I/Ps are in same state.



Boolean Algebra

Commutative Law

i) $A+B = B+A$

ii) $A \cdot B = B \cdot A$

Associative Law

i) $A+(B+C) = (A+B)+C$

ii) $A \cdot (B \cdot C) = (A \cdot B) \cdot C$

Distributive Law

i) $A \cdot (B+C) = A \cdot B + A \cdot C$

Complementary law.

i) $\overline{\overline{A}} = A$

Law for OR Operation

i) $1+A = 1$

ii) $0+A = A$

iii) $A+A = A$

iv) $A+\overline{A} = 1$

v) $\overline{A}+\overline{A} = \overline{A}$

Laws for AND-Operation

i) $A \cdot 0 = 0$

ii) $A \cdot 1 = A$

iii) $A \cdot A = A$

iv) $A \cdot \overline{A} = 0$

v) $\overline{A} \cdot \overline{A} = \overline{A}$

vi) $\overline{A} \cdot 0 = 0$

vii) $\overline{A} \cdot 1 = \overline{A}$

(7) Absorption Law

i) $A+AB = A(1+B) = A$

ii) $A+\overline{A}B = A(1+B)+AB$
$= A+AB+\overline{A}B$
$= A+(A+\overline{A})B = A+B$

iii) $\overline{A}+AB = \overline{A}(1+B)+A \cdot B$
$= \overline{A}+\overline{A}B+AB$
$= \overline{A}+B(A+\overline{A})$
$= \overline{A}+B$

iv) $(A+B)(A+C)$
$= A \cdot A + A \cdot C + A \cdot B + B \cdot C$
$= A(1+C)+A \cdot B + B \cdot C$
$= A + AB + BC$
$= A(1+B)+BC$
$= A+BC$

(8) De-Morgan's Law.

i) $\overline{A+B} = \overline{A} \cdot \overline{B}$

ii) $\overline{A \cdot B} = \overline{A}+\overline{B}$

Minterm

Minterm is the product term in which each variable is present in either in compliment form or ~~non~~ complement form.

A	B	C	Minterm.
0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	$\bar{A}\bar{B}C$
0	1	0	$\bar{A}B\bar{C}$
0	1	1	$\bar{A}BC$
1	0	0	$A\bar{B}\bar{C}$
1	0	1	$A\bar{B}C$
1	1	0	$AB\bar{C}$
1	1	1	ABC

1) Minterm produce '1' (High state) for complementary combination.

2) Minterm produce '0' (low state) from other combinations

Maxterm

1) Max term produce '0' (low state) for complement combinations.

2) Maxterm produce '1' (High state) from other combination

A	B	C	Maxterm
0	0	0	$A+B+C$
0	0	1	$A+B+\bar{C}$
0	1	0	$A+\bar{B}+C$
0	1	1	$A+\bar{B}+\bar{C}$
1	0	0	$\bar{A}+B+C$
1	0	1	$\bar{A}+B+\bar{C}$
1	1	0	$\bar{A}+\bar{B}+C$
1	1	1	$\bar{A}+\bar{B}+\bar{C}$

Maxterm is the sum term in which all each variable are present either in compliment form or un-compliment form.

Sum of Product

Sum of product term is the sum of all product or sum of all product terms is called SOP form.

Ex - $A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC$.

If the expression is $A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC$

Basic formulae - $(\bar{x}+x) = 1$.

then $ABC + \bar{A}BC + \bar{A}B(\bar{C}+\bar{C})$

$111 + 011 + 010$.

Product of Sum

Product of all sum terms or maxterms is called POS or Product of Sum.

001	011	100
~~A+B+C~~	~~A+B+C~~	$\bar{A}+B+C$
$A+B+\bar{C}$	$A+\bar{B}+\bar{C}$	$\bar{A}+B+C$

Basic Formulae.

POS $A \cdot \bar{A} = 0$.

SOP $A+\bar{A} = 1$.

If the expression is $(A+B+\bar{C}) \cdot (A+\bar{B}+\bar{C}) \cdot (\bar{A}+B$

$(A+B+\bar{C}) \cdot (A+\bar{B}+\bar{C}) \cdot (\bar{A}+B+C\bar{C})$.

Design NOR gate using only NAND gate.

2.2.07

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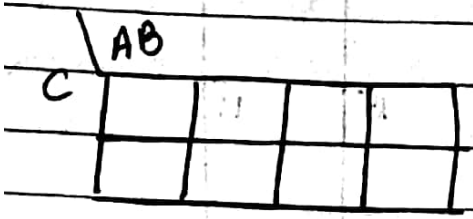
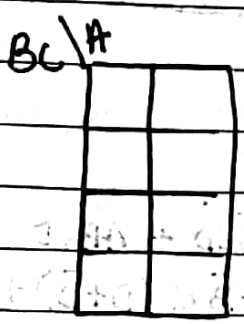
Karnaugh Map.

2^n Variable

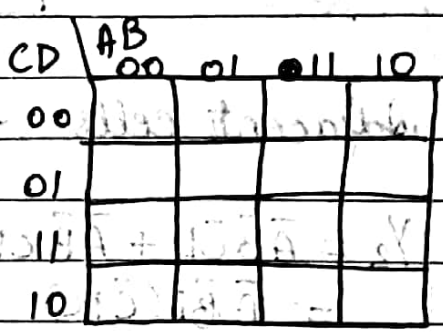


Leftmost + Rightmost
Uppermost + Lowermost

Or



Adjacent cells



ABC
011
3

ABC
010
2

m - Minterm
M - Maxterm.

$1\times2^2+0\times2^1+1\times2^0=5$

$4+0+1=5$

$Y = \Sigma (m_1, m_3, m_{10}, m_{11}, m_{14}, m_{15})$
using K-map.

000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

$A\bar{B}CD + \bar{A}\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + ABC\bar{D} + \bar{A}\bar{B}CD + ABCD$

1011 ◆ 0011 101D 0011 0001 111D

11 3 10 1 14

1111

15

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Adjacent cells - 10, 11, 14, 15

$Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$

$= \bar{A}\bar{B}D(\bar{C}+C)$

$Y_2 = \bar{A}\bar{B}D$

$Y_1 = A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + ABC\bar{D} +$

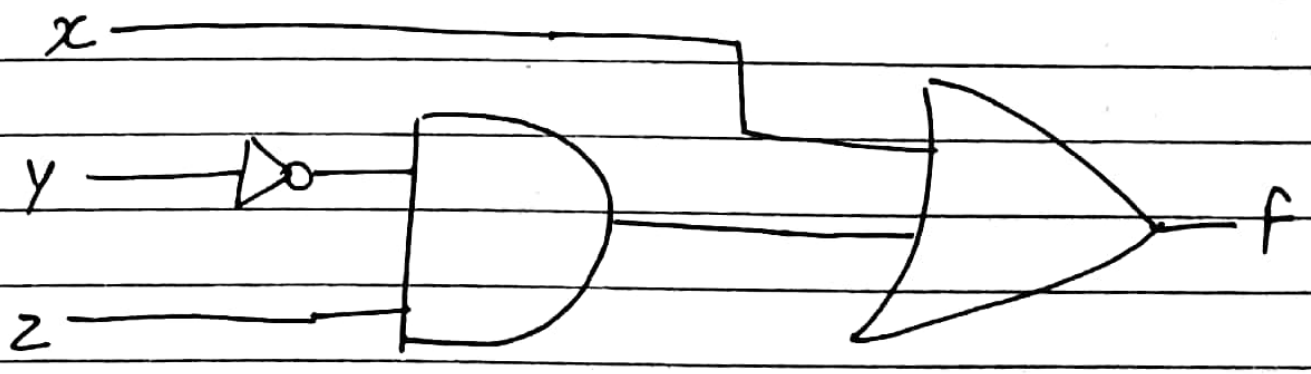
$= A\bar{B}C(D+\bar{D}) + ABC(D+$

$= A\bar{B}C + ABC = AC(\bar{B}+$

To represent a function in a truth table we need a list of 2^n combinations of the n binary function variables.

Ex -

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



Logic diagram

Multiplexers

Multiplexing:

It is the process of transmitting a large no. of information over a single line.

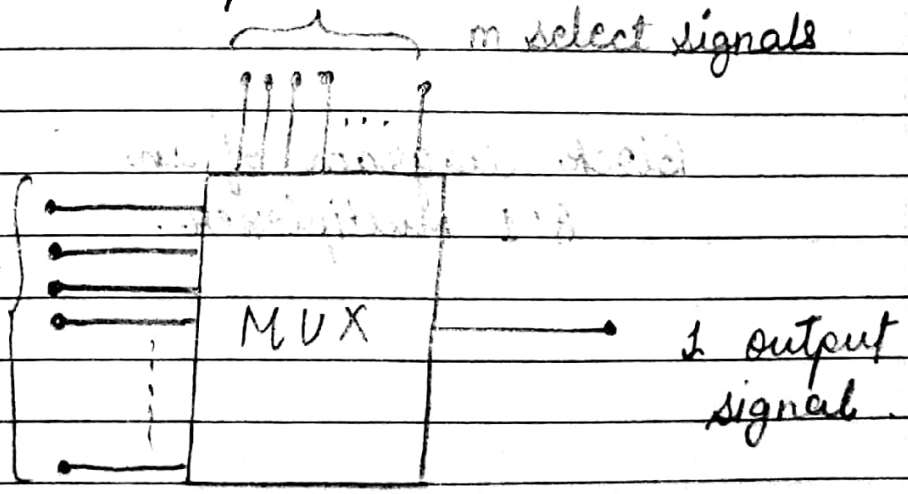
Multiplexer:

A digital multiplexer (MUX) is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line.
It is also called a data selector since it selects one of many inputs and steers the info. to the output.
It has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines.

n = no. of input lines

$n = 2^m$

where 'm' is select lines required to select one of the n input lines.

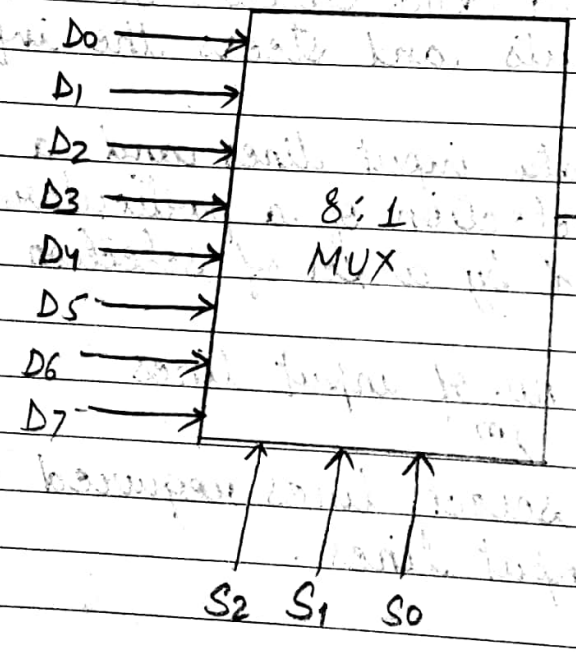


Basic 8 to 1 Multiplexer

An 8 to 1 multiplexer consists of 8 data input D_0 to D_7, three input select lines and a single output line Y.

Depending on the select lines combination, mux decodes the inputs.

Since the no. of data bits given to the mux are 8 then 3 bits ($2^3 = 8$) are needed to select one of the eight data bits.



Block diagram of an 8:1 Multiplexer.

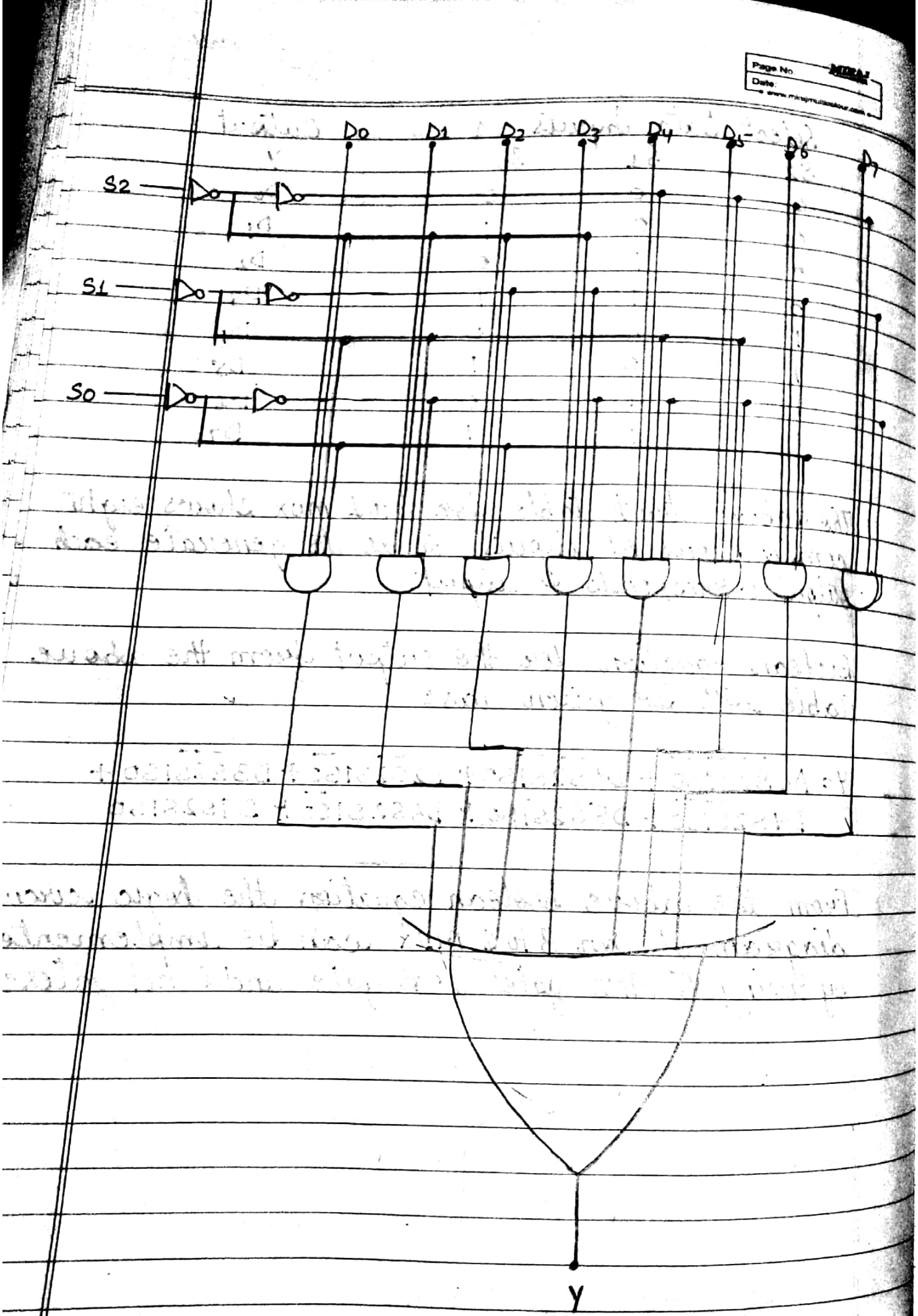
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

The above truth table for 8 to 1 mux shows eight combinations of inputs, so as to generate each output corresponds to input.

Boolean equation for the output from the above table will be given as:

$$Y = D_0 \bar{S_2} \bar{S_1} \bar{S_0} + D_1 \bar{S_2} S_1 \bar{S_0} + D_2 \bar{S_2} S_1 \bar{S_0} + D_3 \bar{S_2} S_1 S_0 + D_4 S_2 \bar{S_1} \bar{S_0} + D_5 S_2 \bar{S_1} S_0 + D_6 S_2 S_1 \bar{S_0} + D_7 S_2 S_1 S_0$$

From the above boolean equation the logic circuit diagram of an 8 to 1 MUX can be implemented by using 8 AND gates 1 OR gate and 6 not gates:



IC 74151 - 8 to 1 Multiplexer

IC74151 is an 8 to 1 multiplexer with eight data input (D_0-D_7), three select input lines (S_2-S_0) and a single output (Y).

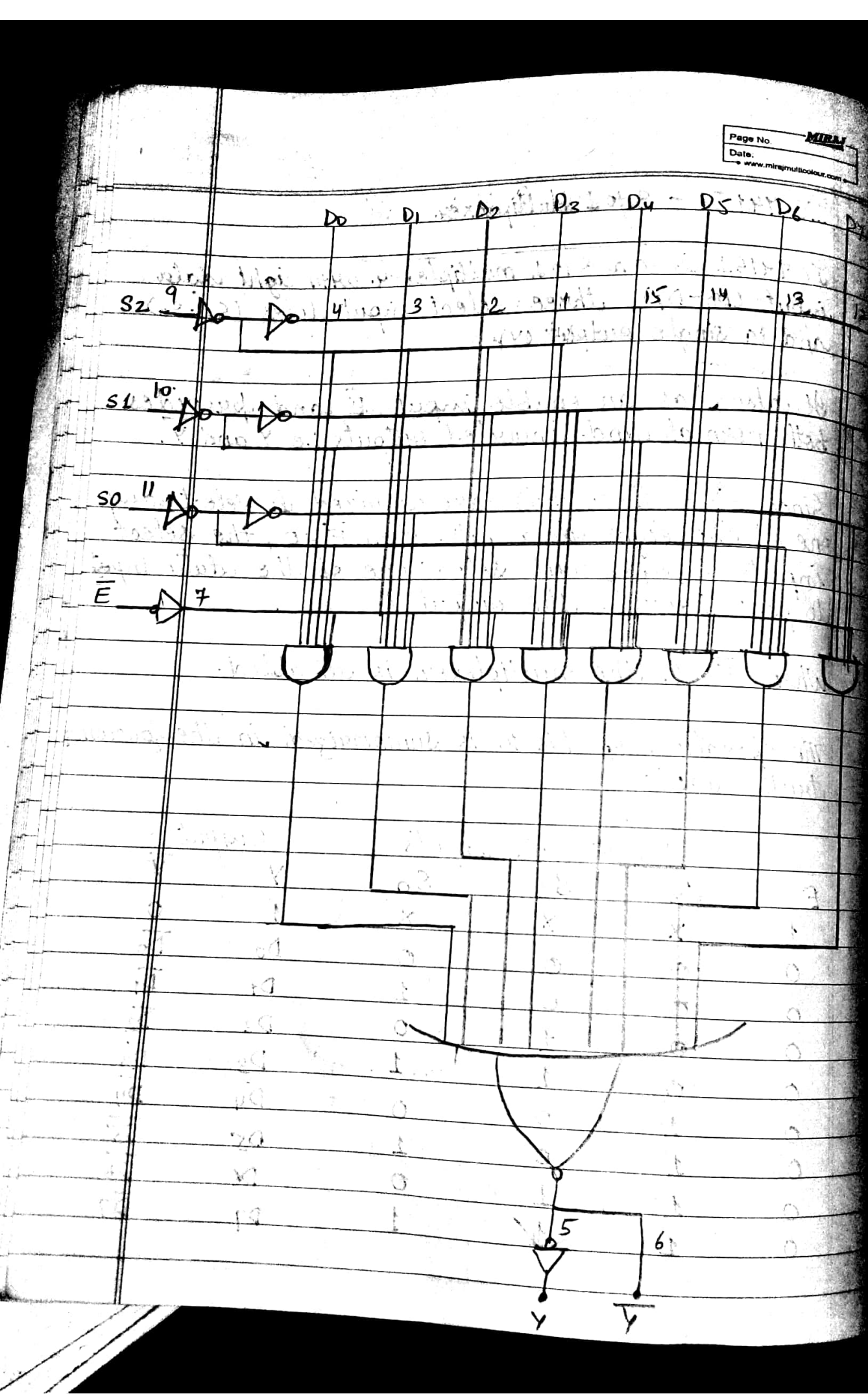
It also has an enable input $\overline{E}$ and provides both normal and inverted outputs i.e Y and $\overline{Y}$.

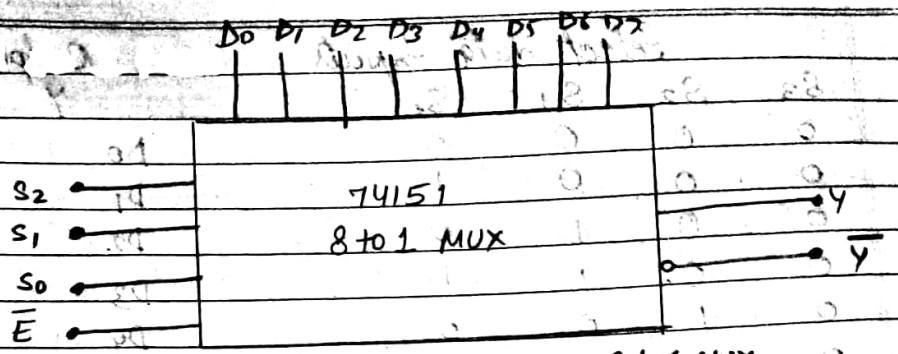
Since $2^3=8$ three bits are required to select any one of the eight data bits. When $\overline{E}=0$, the select inputs $S_2 S_1 S_0$ will select one of the data input to pass through the output Y.

When $\overline{E}=1$, the multiplexer is disabled.

The operation of this IC is summarized in the following truth table.

Select Data Inputs				Output	
E	S_2	S_1	S_0	Y	$\overline{Y}$
1	X	X	X	1	0
0	0	0	0	D_0	$\overline{D_0}$
0	0	0	1	D_1	$\overline{D_1}$
0	0	1	0	D_2	$\overline{D_2}$
0	0	1	1	D_3	$\overline{D_3}$
0	1	0	0	D_4	$\overline{D_4}$
0	1	0	1	D_5	$\overline{D_5}$
0	1	1	0	D_6	$\overline{D_6}$
0	1	1	1	D_7	$\overline{D_7}$





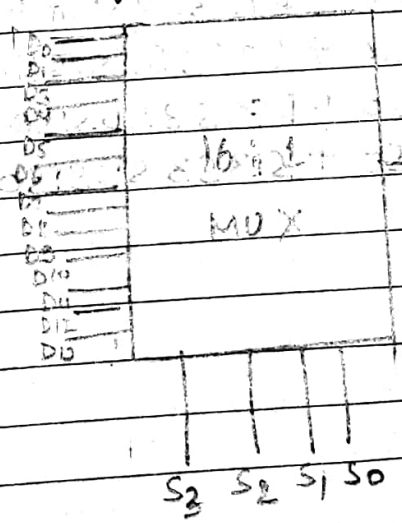
Logic Symbol of IC 74151 - 8 to 1 MUX

16 to 1 Multiplexer

A 16 to 1 multiplexer is consist of 16 data inputs D_0 to D_{15}, four input select lines and a single output line Y.

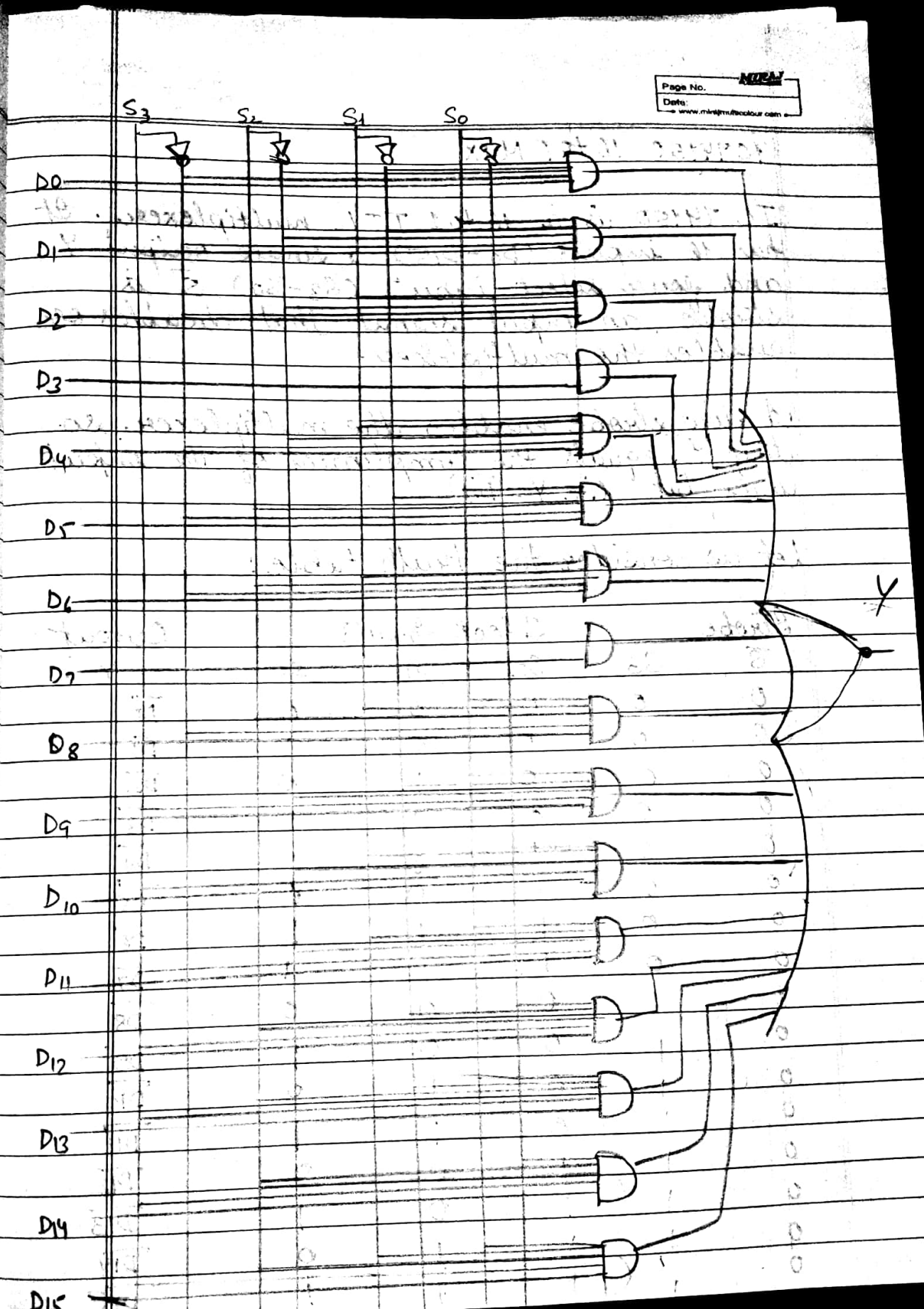
Depending on the select lines combination, mux decodes the inputs.

Since the no. of data bits given to the MUX are 16 then 4 bit ($2^4 = 16$) are needed to select one of the ~~eight~~ 16 data bits.



Select data Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7
1	0	0	0	D_8
1	0	0	1	D_9
1	0	1	0	D_{10}
1	0	1	1	D_{11}
1	1	0	0	D_{12}
1	1	0	1	D_{13}
1	1	1	0	D_{14}
1	1	1	1	D_{15}

$$Y = D_0\bar{S_3}\bar{S_2}\bar{S_1}\bar{S_0} + D_1\bar{S_3}\bar{S_2}\bar{S_1}S_0 + D_2\bar{S_3}\bar{S_2}S_1\bar{S_0} + D_3\bar{S_3}\bar{S_2}S_1S_0 + D_4S_3\bar{S_2}\bar{S_1}\bar{S_0} + D_5S_3\bar{S_2}\bar{S_1}S_0 + D_6S_3S_2\bar{S_1}\bar{S_0} + D_7S_3S_2\bar{S_1}S_0 + D_8S_3S_2S_1\bar{S_0} + D_9S_3S_2S_1S_0 + D_{10}S_3SDS_1S_0 + D_{11}S_3S_2S_1S_0 + D_{12}S_3S_2S_1S_0 + S_{13}S_3SDS_1S_0$$



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IC 74150 16 to 1 Mux

IC 74150 is a 16 to 1 TTL multiplexer. It has 16 inputs ($D_0 - D_{15}$) a single output Y and four select inputs ($S_3 - S_0$). $\overline{S}$ is strobe, an input signal that disables or enables the multiplexer.

A low strobe enables the multiplexer so that Y equals the compliment of the input data bit (i.e $Y = \overline{D_n}$)

Let us consider the truth table:

Strobe	Select Inputs				Output
$\overline{S}$	S_3	S_2	S_1	S_0	Y
0	0	0	0	0	$\overline{D_0}$
0	0	0	0	1	$\overline{D_1}$
0	0	0	1	0	$\overline{D_2}$
0	0	0	1	1	$\overline{D_3}$
0	0	1	0	0	$\overline{D_4}$
0	0	1	0	1	$\overline{D_5}$
0	0	1	1	0	$\overline{D_6}$
0	0	1	1	1	$\overline{D_7}$
0	1	0	0	0	$\overline{D_8}$
0	1	0	0	1	$\overline{D_9}$
0	1	0	1	0	$\overline{D_{10}}$
0	1	0	1	1	$\overline{D_{11}}$
0	1	1	0	0	$\overline{D_{12}}$
0	1	1	0	1	$\overline{D_{13}}$
0	1	1	1	0	$\overline{D_{14}}$
0	1	1	1	1	$\overline{D_{15}}$

L	X	X	X	X	L

74150 : MUX

D_7	1	24	V_{cc}
D_6	2	23	D_8
D_5	3	22	D_9
D_4	4	21	D_{10}
D_3	5	20	D_{11}
D_2	6	19	D_{12}
D_1	7	18	D_{13}
D_0	8	17	D_{14}
Strobe	9	16	D_{15}
$\overline{Y}$	10	15	S_0
S_3	11	14	S_1
Gnd	12	13	S_2

Simbom

output Y

output Y

D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9 D_{10} D_{11} D_{12} D_{13} D_{14} D_{15}

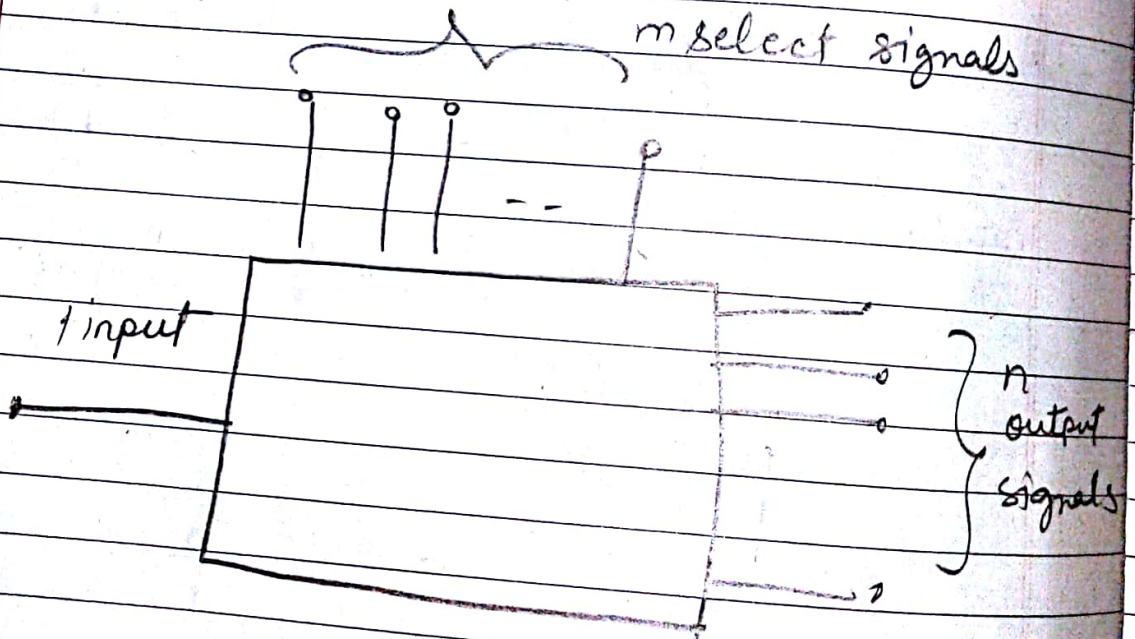
De-multiplexer

Demultiplexing:

It is the process of taking information from one input and transmitting the same over one of several outputs.

Demultiplexer:

A demultiplexer is a logic circuit that receives information on a single input and transmit the same information over one of several (2^m) output lines.



1 to 8 Demultiplexer

A 1 to 8 demultiplexer has a single input (D) eight outputs (Y_0 to Y_7) and three select inputs (S_2, S_1 and S_0).

It distributes one input line to eight output lines based on the select inputs.

Data Input	Select Input			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

$$Y_0 = \overline{S_2}\,\overline{S_1}\,\overline{S_0}D$$
$$Y_1 = \overline{S_2}\,\overline{S_1}S_0D$$
$$Y_2 = \overline{S_2}S_1\overline{S_0}D$$
$$Y_3 = \overline{S_2}S_1S_0D$$
$$Y_4 = S_2\overline{S_1}\,\overline{S_0}D$$
$$Y_5 = S_2\overline{S_1}S_0D$$
$$Y_6 = S_2S_1\overline{S_0}D$$
$$Y_7 = S_2S_1S_0D$$

Now using the above expression the logic diagram of 1 to 8 demux can be drawn as follows.

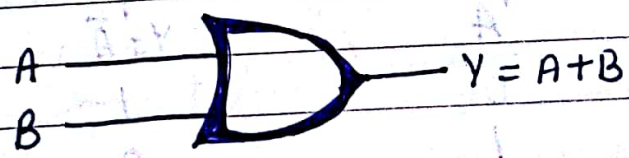
Logic Gates

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. i.e represented in a tabular form called as truth table. In other words, A logic gate is an electronic circuit which makes logical decision. These are the building blocks of hardware which are available in the form of various IC families. Each gate has a distinct logic symbol and its operation can be described by means of an algebraic function.

OR Gate:

The OR Gate is a digital logic gate that implements logical disjunction - it is i.e A high output (1) result if one or both the inputs to the gate are high (1). If neither inputs is high, a low output (0) results.

Input		Output
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1



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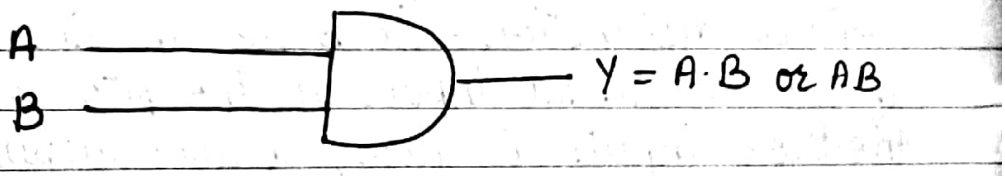
And Gate:

The And Gate is a basic digital logic gate that implements logical conjunction i.e A high output (1) results only if both the inputs to the AND gate are High (1). If neither or only one input to the AND gate is High, a low output (0) results

Input		output
A	B	Y. A·B
0	0	0
0	1	0
1	0	0
1	1	1



Not Gate:

An Inverter or Not gate is a logic gate which implements logical negation. Its main function is to invert the input signal applied. If the applied input is low then the output becomes high and vice versa.

Input	output
A	$Y = \bar{A}$
0	1
1	0

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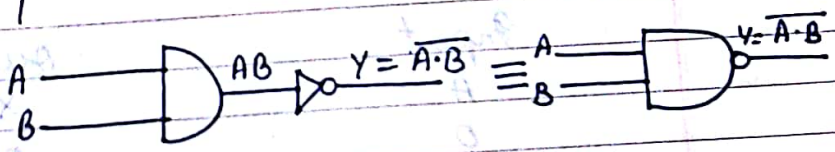
NAND Gate

Nand Gate or Negative AND is a logic gate which produce an output which is false only if all its inputs are true; thus its output is complement to that of And Gate.

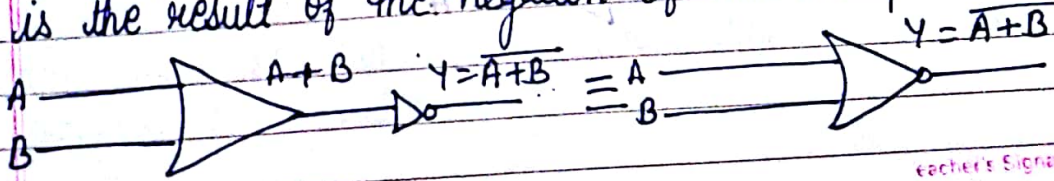
A low (0) output results only if both the inputs to the gate are High (1); if one or both inputs are low (0), a high (1) output results. It is made using transistors and junction diodes.

Input		output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



NOR Gate

The NOR gate is digital logic gate that implements logical NOR i.e A high output (1) results if both the input to the gate are low (0); if one or both input is high (1); A low output (0) results. It is the result of the negation of the OR operator.



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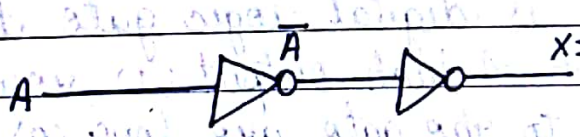
Input		Output
A	B	$Y = \bar{A} + B$
0	0	1
0	1	0
1	0	0
1	1	0

Buffer Gate:

A buffer gate, is a basic logic gate that passes its inputs, unchanged to its output. Its behaviour is opposite of a Not gate. The main purpose of a buffer gate is to regenerate the input, usually using strong high and a strong low. It has one input and one output; its output always equals its inputs. It is also used to increase the propogation delay of circuits by driving the large capacitive loads.

Input	output
A	X
0	0
1	1



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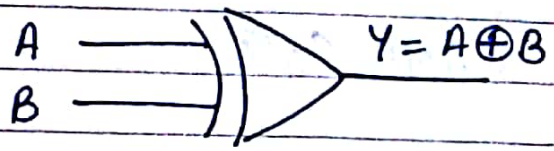
XOR Gate :

The XOR Gate is a digital logic gate that gives a true (1 | High) output when the number of true inputs is odd. That is A true output results if one, and only one, of the inputs to the gate is true. If both the input are false (0 | low) or both are true, a false output results.

It represents the inequality function i.e the output is true if the inputs are not alike otherwise the output is false.



Input		Output
A	B	Y = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

XNOR Gate

The XNOR gate is a digital logic gate whose function is the logical compliment of the exclusive OR gate. The two input version implements logical equality, behaving as, A high output (1) results if both of inputs to the gate are the same. If one but not both inputs are high (1), a low output (0) results.

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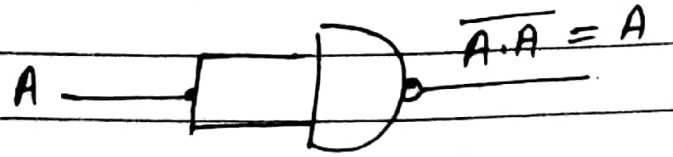
NAND Gate

1) NOR

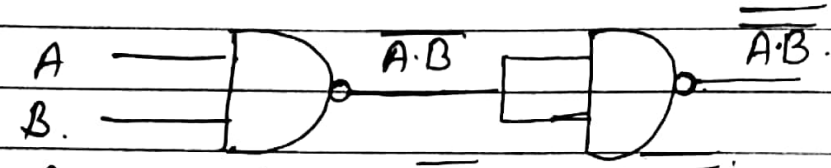
$(A \cdot 1)' = \bar{A}$



$\bar{A} = \overline{A \cdot A} = \bar{A}$

A	$\overline{A \cdot A}$	$\bar{A}$
0	1	1
1	0	0

2)



A	B	$\overline{A \cdot B}$	$\overline{\overline{A \cdot B}}$	$A \cdot B$
0	0	1	0	0
0	1	1	0	0
1	0	1	0	0
1	1	0	1	1

$\overline{A \cdot B} = \overline{A} + \overline{B}$

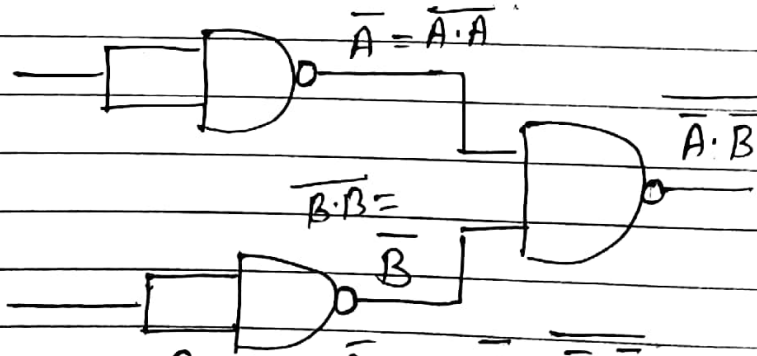
$= AB$

Double Complement law

3)

$\bar{A} = \overline{A \cdot A}$

$\bar{B} = \overline{B \cdot B}$



$\overline{\bar{A} \cdot \bar{B}} = \overline{\overline{A} + \overline{B}}$

$= A + B$

Demorgan's law

Double Complement law

A	B	$\bar{A}$	$\bar{B}$	$\overline{\bar{A} \cdot \bar{B}}$	$A + B$
0	0	1	1	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	1	0	0	1	1

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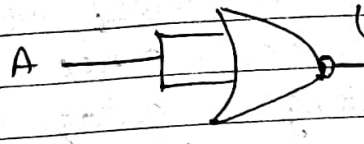
OR Gate

$(A+0)' = A$.

$(A+A)' = A'$

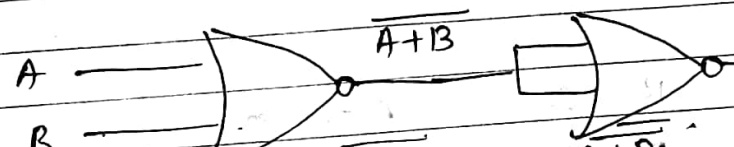
$\overline{A+A} = \overline{A}$

1) NOR.



A	$\overline{A+A}$	$\overline{A}$
0	1	1
1	0	0

2) OR.

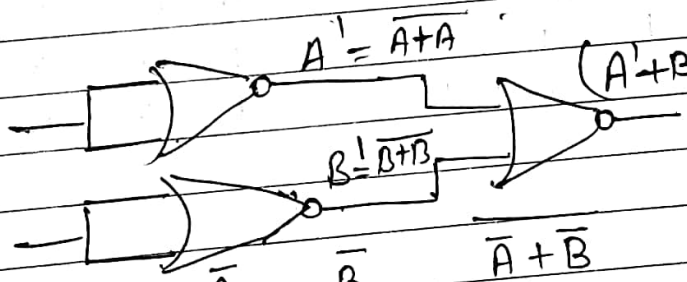


$\overline{\overline{A+B}} = A+B$

A	B	$\overline{A+B}$	$\overline{\overline{A+B}}$	$A+B$
0	0	1	0	0
0	1	0	1	1
1	0	0	1	1
1	1	0	1	1

Double complement law

3) AND



$\overline{A+A} = \overline{A}$

$\overline{B+B} = \overline{B}$

$\overline{\overline{A}+\overline{B}} = \overline{A \cdot B}$

$= A \cdot B$

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	$A \cdot B$
0	0	1	1	0	0
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	1	1

Demorgan law

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K- Map.

K- map is a method to simplify boolean algebra expression. It reduces the need for extensive calculation by taking advantage of human's pattern recognition capablity

It is a pictorial ~~art~~ method used to minimize Boolean expression without having to use boolean algebra theorem and equation manipulation

A	B	C	A-B-C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

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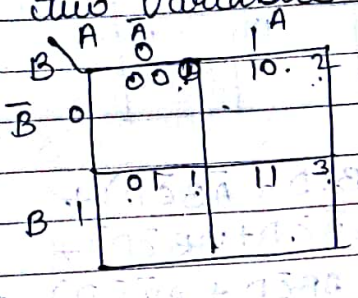
multiplexers. K-Map.

K-Map is a pictorial method to minimize boolean expression without having to use boolean Algebra theorem and equation manipulation.

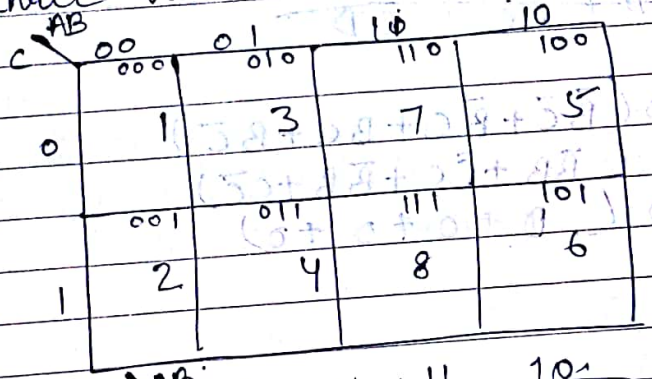
Using two variables

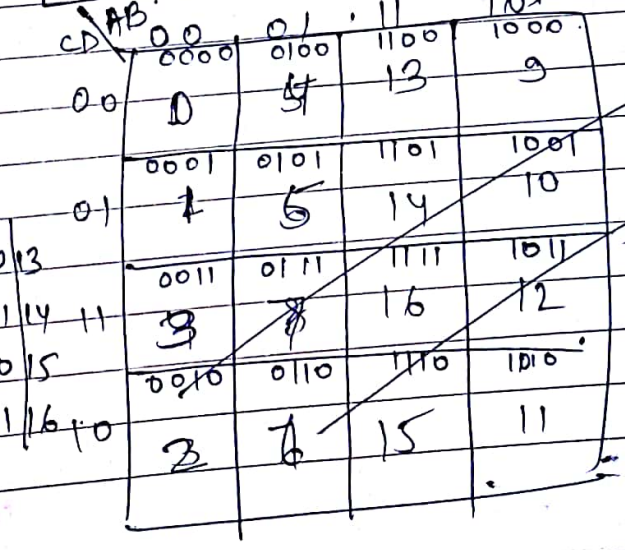


$Y = \bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB.$

000
001
010
011

Using three variables





0000 1
0001 2
0010 3
0011 4
0100 5
0101 6
0110 7
0111 8
1000 9
1001 10
1010 11
1011 12
1100 13
1101 14
1110 15
1111 16

0000 1
0001 2
0010 3
0011 4
0100 5
0101 6
0110 7
0111 8
1000 9
1001 10
1010 11
1011 12
1100 13
1101 14
1110 15
1111 16

on circuit
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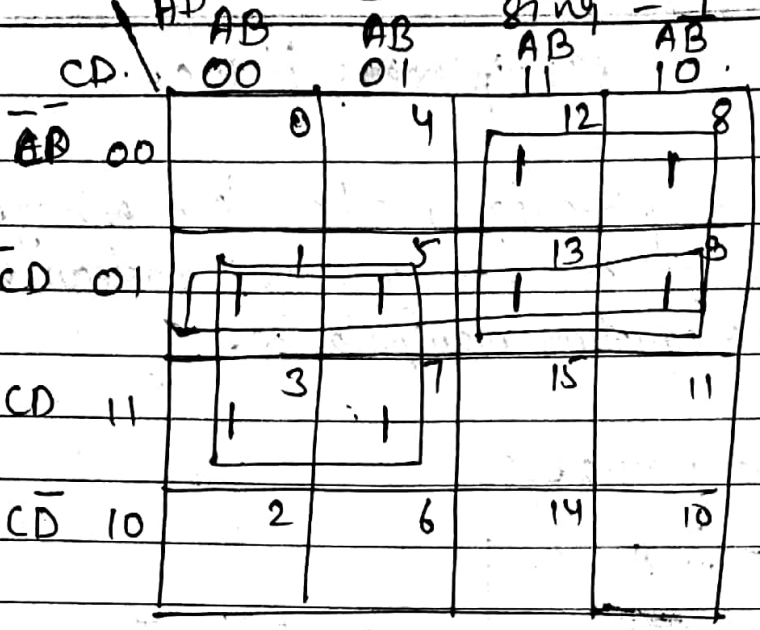

$= (\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}BCD + \bar{A}B\bar{C}D) +$
$(AB\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}D) +$
$(\bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + AB\bar{C}D + A\bar{B}\bar{C}D)$

$= \bar{A}D + A\bar{C} + \bar{C}D$

$= \bar{A}D(\bar{B}\bar{C} + \bar{B}C + BC + B\bar{C})$
$\bar{A}D(\bar{B}B + \bar{C}C + \bar{B}B + C\bar{C})$
$\bar{A}D(D + 0 + 0 + 0)$

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SOP - Minal.
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Minterm-
A product term containing all the K variables of the function in either complemented or uncomplemented form is called a minterm.

A	B	C	Minterm
0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	$\bar{A}\bar{B}C$
0	1	0	$\bar{A}B\bar{C}$
0	1	1	$\bar{A}BC$
1	0	0	$A\bar{B}\bar{C}$
1	0	1	$A\bar{B}C$
1	1	0	$AB\bar{C}$
1	1	1	ABC

Maxterm.
A sum term containing all 'K' variable of the function in either complemented or uncomplemented form is called a Maxterm.

A	B	C	Maxterm.
0	0	0	$A+B+C$
0	0	1	$A+B+\bar{C}$
0	1	0	$A+\bar{B}+C$
0	1	1	$A+\bar{B}+\bar{C}$
1	0	0	$\bar{A}+B+C$
1	0	1	$\bar{A}+B+\bar{C}$
1	1	0	$\bar{A}+\bar{B}+C$
1	1	1	$\bar{A}+\bar{B}+\bar{C}$

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